**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| Application No.: | 10/790,689 |
| Filing Date: | March 3, 2004 |
| Applicant: | Pierte Roo |
| Group Art Unit: | 2611 |
| Examiner: | Siu M. Lee |
| Title: | SYSTEM AND METHOD FOR REDUCING ELECTROMAGNETIC INTERFERENCE AND GROUND BOUNCE IN AN INFORMATION COMMUNICATION SYSTEM BY CONTROLLING PHASE OF CLOCK SIGNALS AMONG A PLURALITY OF INFORMATION COMMUNICATION DEVICES |
| Attorney Docket: | MP0304 |

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

## DECLARATION UNDER 37 C.F.R. § 1.131

I, Pierte Roo, hereby declare as follows:

1. I am the inventor of the subject matter claimed in U.S. Application No. 10/790,689 ("the Application").

2. I understand that U.S. Patent No. 6,946,870 by Austin Lesea, entitled "Control of Simultaneous Switch Noise from Multiple Outputs" ("Lesea"), has been cited as prior art against the Application. That in a Non-Final Office Action dated January 22, 2008, all claims were

rejected under 35 U.S.C. § 102(e) as being anticipated by Lesea, or as being unpatentable over Lesea in combination with one or more other references.

3. Lesea issued from U.S. Application No. 10/691,146 filed on October 21, 2003.

4. That the materials attached at Exhibits A and B have dates that are blacked out, which pre-date October 21, 2003. Attention is respectfully drawn to the redacted version of the project notes, attached as Exhibit B (Pages 1-6). The redacted date on Page 1 is earlier than October 21, 2003, which is the effective date of Lesea.

5. Prior to October 21, 2003, the invention which is the subject matter of the Application was conceived in the United States and reduced to practice, as evidenced by the attached Exhibits A and B submitted herewith.

6. That Exhibit A is a letter sent prior to October 21, 2003 from the assignee of the Application to a local patent counsel requesting the preparation of the Application, which shows that we were diligent in further developing my invention, and providing assistance to the patent counsel in preparing and filing the Application from a time prior to the filing date of Lesea until the March 3, 2004 filing data of the Application. Accordingly, the invention has never been abandoned, suppressed, or concealed.

7. I am the author of the project notes attached as Exhibit B.

8. The attached project notes evidence of Exhibit B is conception and reduction to practice of subject matter included within claims 1-108. Essentially, independent claim 1 recites an information communication system that includes a plurality of information communication devices. Each of the plurality of information communication devices is responsive to a respective information communication clock signal. Each information communication clock signal of each of the plurality of information communication devices is associated with a

common reference clock signal. The system also includes a phase controller that is responsive to the common reference clock signal. The phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount. Claims 14, 27, 37, 48, 59, 65, 78, 91 and 100 recite similar subject matter. Claims 2-13, 15-26, 28-36, 38-47, 49-58, 60-64, 66-77, 79-90, 92-99 and 101-108 ultimately depend from claims 1, 14, 27, 37, 48, 59, 65, 78, 91 and 100.

9. The plurality of information communication devices are shown as ports at A on Page 5 of the project notes. Each port receives a respective clock signal, as seen on Page 5 at B of the project notes. Each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (example shown at C on Page 3 of the project notes, where a reference clock signal refclk is input and different/offset clock signals are output following each inverter). A phase controller is seen, for example, at D on Page 5 of the project notes, as a plurality of inverters delaying an input clock signal to provide respective shifted clock signals to respective ports. The phase controller (seen at D on Page 5 of the project notes) alters the phase by an amount, such as 90 degrees, as shown at E on Page 1 of the project notes.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are being made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application or any patent issued thereon.

Dated: 1/6/2009

Pierte Roo

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**EXHIBIT A**

[redacted]

Via Facsimile (202) 298-7570
Confirmation Via Federal Express
Richard P. Bauer, Esq.
Katten Muchin Zavis
1025 Thomas Jefferson St., NW
Washington, DC 20007-5201

Re: New U.S. Patent Application: Gigabit Transmit Clocking for Reducing EMI and Supply Bounce
Our Docket No.: MP0304
Your Reference No.:
Requirements: Prepare new patent application
Marvell Target Date: November 14, 2003

Dear Rick:

We would like you to prepare a patent application directed to the above-identified invention by no later than November 14, 2003. Please find enclosed documents describing the invention along with a videotape of an invention disclosure interview.

The inventorship information is as follows:

| Inventor | Citizenship | Address | City | State | Zip | Country |
|---|---|---|---|---|---|---|
| Roo, Pierte | US | 144 Holly Ct. | Mountain View | CA | 94043 | US |

Please review the enclosed materials and before proceeding please provide your estimate as to cost and schedule.

Please also prepare a declaration and assignments as follows.

X Inventor to Marvell Semiconductor Inc.

X Marvell Semiconductor Inc. to Marvell International, Ltd.

The final deliverables will include an electronic version **and a claim tree.**

Please do not hesitate to contact me if you have any questions.

With warmest regards.

Very truly yours,

Amanda J. [illegible] on behalf:

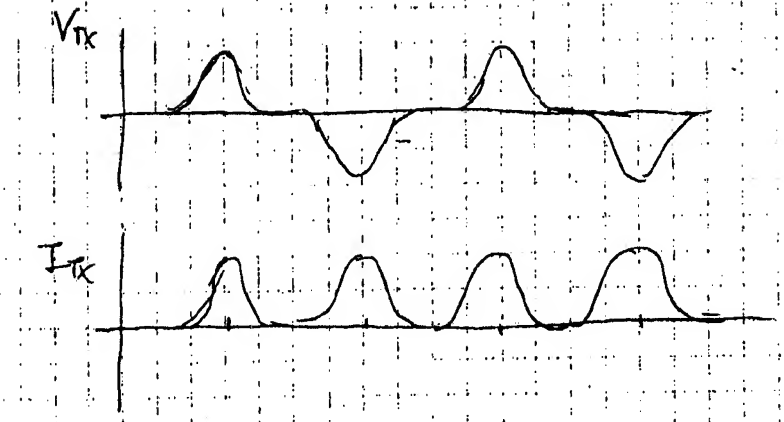
Eric Jantofsky
General Patent Counsel

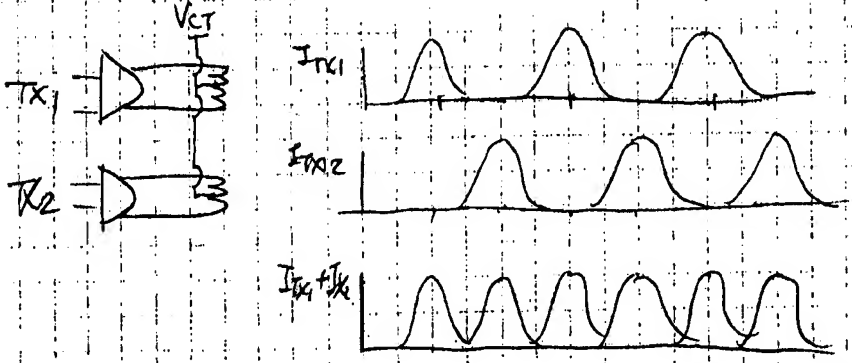
EBJ:ajg
Enclosures: Invention documents (Confirmation Copy)
Video Tape (Confirmation Copy)

**EXHIBIT B**

[redacted]

EMI

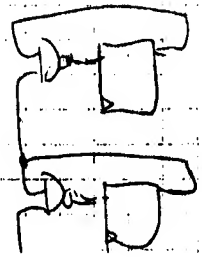


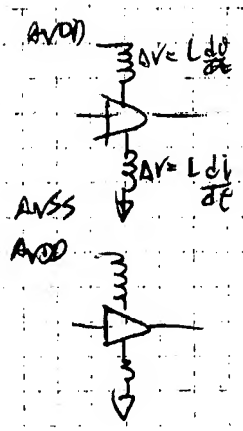




Mixing clock phase

- ✓ local — pair to pair — adjacent pairs.
- ✓ global — port to port — Multi port.
  adjacent phy.

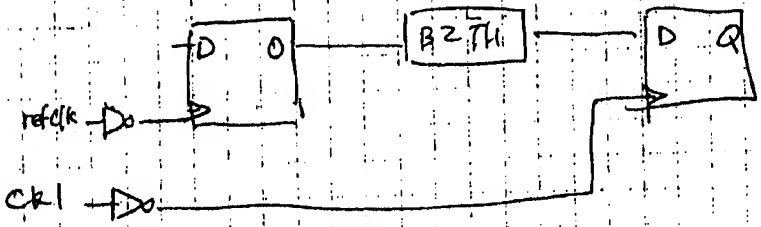
- reduce EMI
- reduce requirement for Common-mode Choke

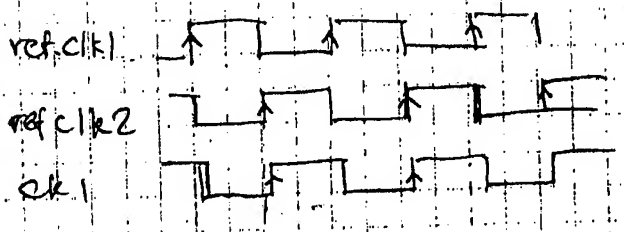




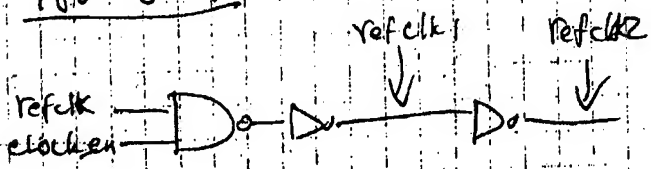

Improvement → - Reduce Power supply bounce
- Reduce EMI (Clock switch a different time).

Decoder



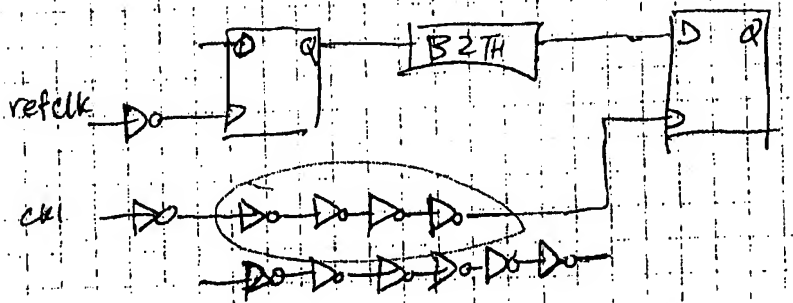




- refclk 2 (inverted from refclk1) is the input to DLL giving 180° shift.



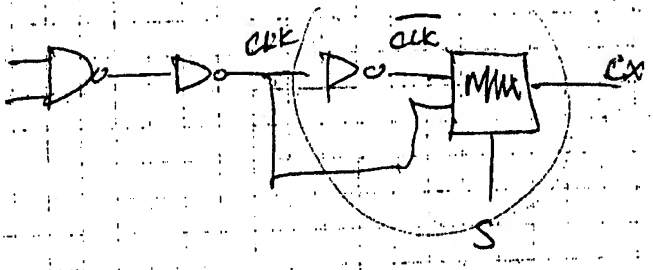

Changes

① change decoder to have clock delay

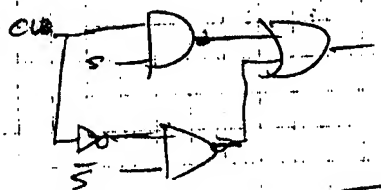


[redacted]

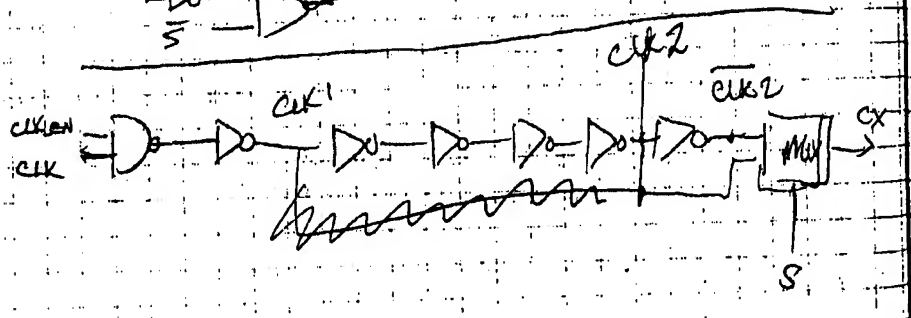
(2) refelk inversion - selectable




$$CX = CLK\,S + \overline{CLK}\,\overline{S}$$




(?)



[redacted]

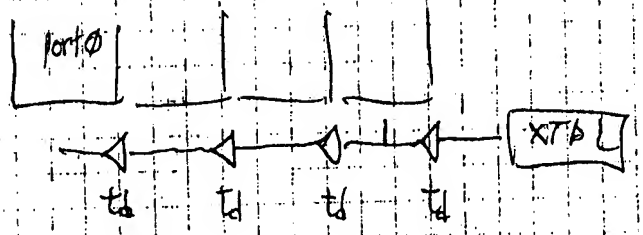
TXDAC phisel

| ch0 | ch1 | ch2 | ch3 |
|---|---|---|---|
| 0 | 180 | 0 | 180 |

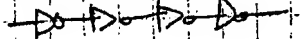
Reg 30_33:15:12 = 1010 (3210)

TBG init

4 ports

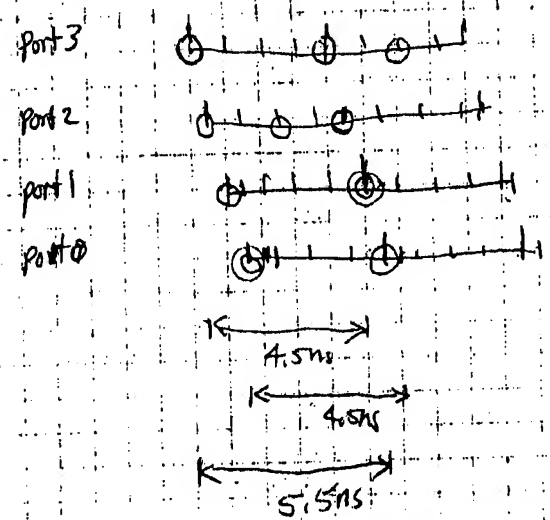



$t_d$ = 4 inverts



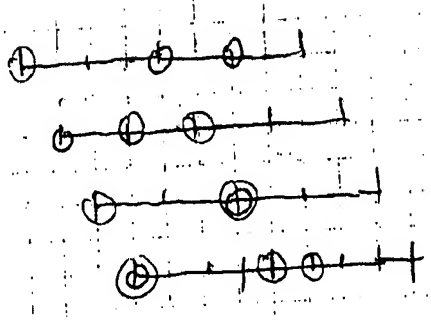
$t_d$ = varies from 0.4ns → 1.0ns

$t_d$ = 0.4ns

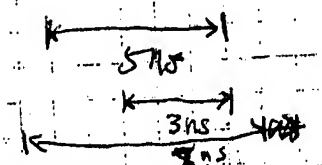



| | | |
|---|---|---|
| 180 | 270° | 0 |
| 0° | 90° | 180 |
| 180° | 180° | 90 |
| 0° | 0° | 180 |

$t_d = 1\,ns$



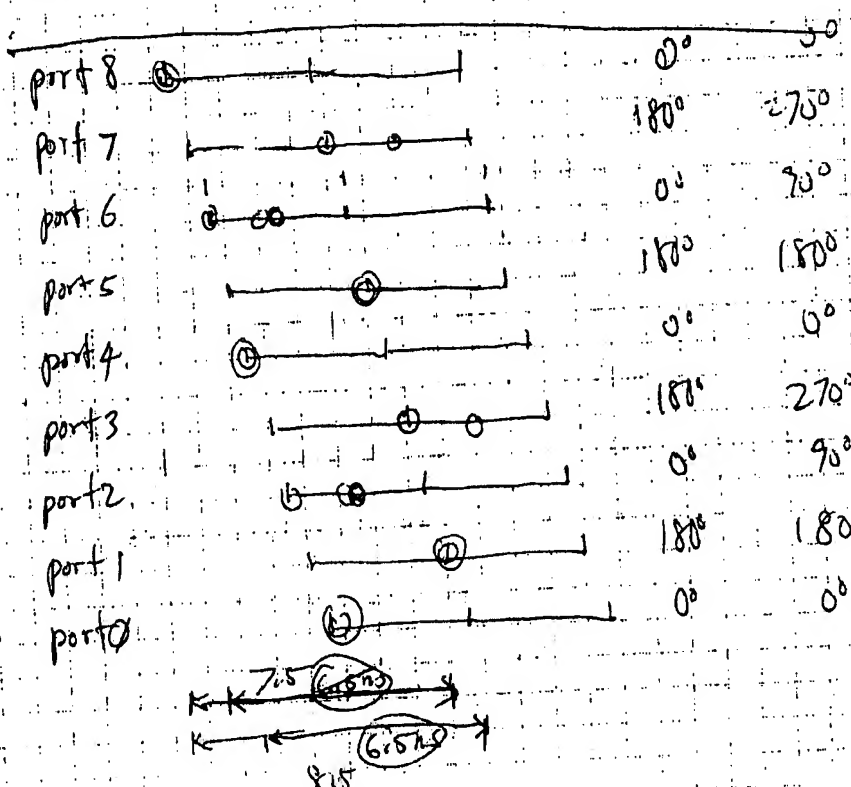

| | | | |
|---|---|---|---|
| | 180° | 270° | 0 |
| | 0° | 90° | 180 |
| | 180° | 180° | 0 |
| | 0° | 0° | 180 |




best choice is 180°, 0°, 180°, 0° (3210)

9 ports

$t_d = 0.5\,ns$




| | | |
|---|---|---|
| 0° | 90° | |
| 180° | 270° | |
| 0° | 90° | |
| 180° | 180° | |
| 0° | 0° | |
| 180° | 270° | |
| 0° | 90° | |
| 180° | 180 | |
| 0° | 0° | |

8.5